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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,138	03/19/2004	Osamu Ichikawa	L8462.04111	6381

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,138	ICHIKAWA, OSAMU	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 19 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/19/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-11 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 3/19/04 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The drawings filed March 19, 2004 are acceptable.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

The abstract of the disclosure is objected to because "an test" should read "a test". Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 1, 4, 7, 8,and 9, are objected to because of the following informalities: "an test" should read "a test". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 - The statement "outputs a signal showing the existence or nonexistence of said faulty cell, and including a pass/fail judgment signal for every bit" is unclear. This can be read as a single output including the pass/fail signal or two separate signals.

Claim 1 also states "a first data storage section, which during an test of said memory, retrieves a signal which has branched from all or a part of Column address signals which are inputted into said memory from said test pattern generating section, and the pass/fail judgment signal for every said bit generated by said comparing section as faulty address data, and during an test of a peripheral logic of said memory, forms a part of a scan chain, and is used for observing an input signal into said memory;" this entire segment of the claim is unclear to the examiner. It is not clear how "...retrieves a signal ... which are inputted " there is no subject verb agreement. It is also unclear what is used for observing an input signal into the memory, because at this point several signals have been mentioned, and the most recent subject was the scan chain.

Claim 1 "to store a state of the presence or absence of a failure corresponding to the existence or nonexistence of said faulty cell" it is unclear here if a "state" is a fail location or address or just flag to indicate a failed cell.

Claim 1 also states "said second data storage section is in a state where said failure exists" this claim language is unclear as to whether the entire storage area is in a fail state or is there is a specific area of the data storage section for the fail state to be flagged. Claim 1 - "first data storage section holds the data retained in said first data storage section" It is unclear to the examiner why this statement is necessary in the claim language. Clarification of the claim language is required.

Claim 4 - The statement "outputs a signal showing the existence or nonexistence of said faulty cell, and including a pass/fail judgment signal for every bit" is unclear. This can be read as a single output including the pass/fail signal or two separate signals.

Claim 4 also states "a first data storage section, which during an test of said memory, retrieves a signal which has branched from all or a part of Column address signals which are inputted into said memory from said test pattern generating section, and the pass/fail judgment signal for every said bit generated by said comparing section as faulty address data, and during an test of a peripheral logic of said memory, forms a part of a scan chain, and is used for observing an input signal into said memory" this entire segment of the claim is unclear to the examiner. It is not clear how "...retrieves a signal ... which are inputted " there is no subject verb agreement. It is also unclear what is used for

observing an input signal into the memory, because at this point several signals have been mentioned, and the most recent subject was the scan chain.

Claim 4 - states "a repair judging section, which receives an input to said first data storage section and an output of retained contents in said first data storage section, and judges that said memory is repairable" The examiner would like to point out that if the repair judging section always judges that the memory is repairable it would not be necessary – it would either judge that the memory is or is not repairable or it would not be necessary.

Claim 4 – it is unclear to the examiner if the faulty cell becomes active when the FAIL signal is received or if the data storage section becomes active. It is also unclear if/how the entire storage section would become active or if there is merely a flag or a signal held in the active position until the test is complete.

Clarification of the claim language is required.

Independent claims 7, 8, and 9, contain the same types of clarity issues. The examiner request the claims be rewritten in a manner which clarifies the subject matter which the applicant regards as his invention.

Dependent claims 2, 3, 5, 6, 10, and 11 inherit the 35 U.S.C. 112, second paragraph issues of the independent claims and will nor be further treated on their merits.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an

application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,4, and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohtani et al. U.S. Patent No. 6,421,286.

As per claims1, 4, and 7-9 Ohtani et al teach the claimed invention (circuit and method) a semiconductor integrated circuit device, being provided with plural memory circuits and a redundancy replacement test circuit. Each of the plural memory circuits includes a normal memory cell array having plural normal memory cells therein and a spare memory cell array having plural spare memory cell rows and plural spare memory cell columns therein. The redundancy replacement test circuit is provided commonly to the plural memory circuits to determine a defective address to be repaired by replacement. The redundancy replacement test circuit includes a self-test circuit and a redundancy analysis circuit. The self-test circuit generates address signals for sequentially selecting memory cells to detect a defective memory cell based on results of comparison between data read out from the memory cells and expected value data. The redundancy analysis circuit determines a defective address on which replacement is to be performed with one of plural spare memory cell rows and plural spare memory cell columns according to an address signal from the self-test circuit and a detection result on the defective memory cell. The redundancy analysis circuit has an address storage circuit, a drive circuit and a determination circuit. The address storage circuit stores a defective address corresponding to a defective memory cell. The drive circuit limits an effective memory space of the address storage circuit according to a capacity of a memory circuit to be tested

among the plural memory circuits and performs data storage into the address storage circuit. The determination circuit determines which of spare memory cell rows and spare memory columns the defective cell is replaced with according to a defective address stored in the address storage circuit. The address storage circuit selectively stores the defective address different from any of already stored detective row addresses and defective column addresses among sequentially detected defective addresses. The address storage circuit preferably includes plural CAM cells (Content Addressable Memory Cells) arranged in matrix. Furthermore, the determination circuit preferably comprises a plurality of replacement determination sections provided correspondingly to respective sequences of replacement steps. Each of the sequences of replacement steps corresponds to a sequence in which defective memory cell rows and defective memory cell columns are sequentially replaced with spare memory cell rows and spare memory cell columns in the memory circuit including the maximum number of spare memory cell rows and spare memory cell columns among the plurality of memory circuits. Each of the plurality of replacement determination sections has a replacement sequence determination circuit and a determination step limit circuit. The replacement sequence determination circuit determines whether repair of defective memory cells is completed before reaching a final step among the sequence of replacement steps. The determination step limit circuit selectively sets one of the replacement steps as the final step according to the number of the spare memory cell rows and the spare memory cell columns belonging to the memory circuit to be tested among the plurality of memory

circuits. Alternatively, the semiconductor integrated circuit device further includes plural select circuits provided correspondingly to respective plural memory circuits and connected in series to each other. Write data to a memory circuit to be tested among the plural memory circuit is transmitted from a self-test circuit by a shifting operation sequentially passing through the plural select circuits. Alternatively, the redundancy replacement test circuit further preferably includes: a first internal address generation circuit for generating an internal address for a test operation according to a capacity of a memory cell array of a memory circuit to be tested among the plural memory circuits. Each memory circuit further includes: a second internal address generation circuit generating an internal address for a test operation on a memory circuit in synchronism with the first internal address generation circuit based on an initial value given from said redundancy replacement circuit.(Column 3 line 35 through column 4 line 48)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,808,947 McClure

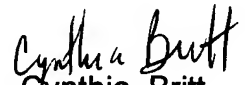
This patent teaches a self repair circuit on a wafer die.

If applicant requires more clarification on the 35 U.S.C. 112 second paragraph rejections of the independent claims above, the examiner is available by telephone . See below.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Cynthia Britt
Examiner
Art Unit 2138

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